CLAIMS

What is Claimed is:

1. A voltage regulator comprising:

an input stage having a first input, a second input, and an output;

a reference voltage circuit coupled to said first input;

an output stage coupled to said second input; and

a gain stage comprising a buffer device and a drive circuit, said buffer device coupled to said output of said input stage and said drive circuit, said drive circuit coupled to said output stage, wherein said buffer device is operable to provide isolation between said input stage and said drive circuit.

2. The voltage regulator of Claim 1, wherein said drive circuit comprises a field effect transistor.

3. The voltage regulator of Claim 1, wherein said drive circuit comprises:

a first transistor coupled to said output stage;

a base current translation circuit; and

a current divide circuit coupled to the first transistor and to said base current translation circuit, wherein said current divide circuit is operable to deliver a portion of a first current of said first transistor to said base current translation circuit; and

wherein said base current translation circuit is operable to deliver to the base of said first transistor a second current.

4. The voltage regulator of Claim 3, wherein said second current is greater in magnitude than a base current of the first transistor.

5. The voltage regulator of Claim 1, further comprising a capacitor coupled to said buffer device and said input stage, and wherein said buffer device comprises a beta of approximately at least 1000.

6. The voltage regulator of Claim 1, further comprising:

an impendence coupled to said second input of the input stage and to said output stage; and

a device coupled to said input stage to provide a substantially constant bias current for said input stage, wherein output dependent current loading effects through said impedance are avoided.

7. The voltage regulator of Claim 1, further comprising a proportional to absolute temperature circuit coupled to said input stage and said gain stage and operable to provide a biasing current that is substantially independent of temperature.

8. A low dropout voltage regulation circuit comprising:

an input comparison stage having an inverting input, a non-inverting input, and an output, said inverting input coupled to an output voltage node;

a bandgap reference voltage circuit coupled to said non-inverting input;

a low dropout output stage coupled to an input voltage node and the output voltage node; and

a gain stage comprising a buffer device and a drive circuit, said buffer device coupled to said output of said input stage and said drive circuit, said drive circuit

coupled to said output stage, wherein said buffer device is operable to provide isolation between said input stage and said drive circuit.

9. The regulation circuit of Claim 8, wherein said buffer device comprises a pnp transistor.

10. The regulation circuit of Claim 8, wherein said drive circuit comprises:

a first transistor coupled to said output stage;

a base current translation circuit; and

a current divide circuit coupled to the first transistor and to said base current translation circuit, wherein said current divide circuit is operable to deliver a portion of a first current of said first transistor to said base current translation circuit; and

wherein said base current translation circuit is operable to deliver to the base of said first transistor a second current that is greater in magnitude than a base current of the first transistor.

11. The voltage regulator of Claim 8, wherein said drive circuit comprises a field effect transistor.

12. The voltage regulator of Claim 8, further comprising:

an impendence coupled to said inverting input of the input comparison stage and to said output stage; and

a transistor coupled to said input comparison stage to provide a substantially constant bias current for said input stage, wherein output dependent current loading effects through said impedance are avoided.

13. The voltage regulator of Claim 8, further comprising:

a biasing device coupled to said input comparison stage and to said output stage, wherein said biasing device is configured to provide a bias current to said input stage that is logarithmically related to an output current of said output stage.

14. The voltage regulator of Claim 8, further comprising:

a biasing device coupled to said input comparison stage and to said output stage, wherein said biasing device is configured to provide a bias current to said input stage that is linearly proportional to an output current of said output stage.

15. A voltage regulation circuit comprising:

an input comparison stage comprising a first pnp transistor and a second pnp transistor, said first pnp transistor coupled to an output voltage node;

a bandgap reference voltage circuit coupled to said second pnp transistor;

an output stage coupled to an input voltage node and the output voltage node; and

a gain stage comprising a third pnp transistor and a drive transistor, said third pnp transistor coupled to said output of said input stage and said drive transistor, said drive transistor coupled to said output device.

16. The voltage regulation circuit of Claim 15, wherein said gain stage further comprises:

mirror transistors coupled to said drive transistor; and

a translation circuit coupled to the mirror transistors;

wherein the mirror transistors are operable to deliver a portion of a first current of said drive transistor to said translation circuit; and

wherein said translation circuit is operable to deliver to the base of said drive transistor a second current that is greater in magnitude than a base current of said drive transistor.

17. The voltage regulation circuit of Claim 16, wherein said translation circuit comprises a first translation transistor coupled to the mirror transistors and a second translation transistor coupled to the base of the drive transistor.

18. The voltage regulator of Claim 17, further comprising a pnp cascode transistor having a base coupled to said first translation transistor and an emitter coupled to said second translation transistor.

19. The voltage regulator of Claim 15, wherein said third pnp transistor is configured as a substantially unity gain buffer.

20. The voltage regulator of Claim 15, further comprising:

an impendence coupled to said first pnp transistor and to said output voltage node; and

a biasing transistor coupled to said input comparison stage to provide a substantially constant bias current for said input stage, wherein output dependent current loading effects through said impedance are avoided.

21. The voltage regulator of Claim 15, further comprising a proportional to absolute temperature circuit coupled to said input stage and said gain stage and operable to provide a biasing current that is substantially independent of temperature.